

## SPECIFICATION

### STRUCTURE OF POWER SUPPLY PATH UTILIZED IN DESIGN OF INTEGRATED CIRCUIT

5

#### BACKGROUND OF THE INVENTION

The present invention relates to a structure of a power supply path utilized in the design of an integrated circuit and more particularly, it relates to a technique of estimating charge and discharge times and power consumption of a part in which a power supply voltage is controlled. When a voltage supplied to a part of an integrated circuit or the whole thereof is controlled, it is necessary to estimate charge and discharge times of the part to be controlled. When performing this estimate, a resistance value and a stray capacitance value of a main line, and a resistance value and a stray capacitance value of an outgoing line are comprehensively considered in order to calculate the charge and discharge times.

The estimate of the charge and discharge times is made after cell arrangement is completed and the power supply path is determined. Even when configurations and dimensions of the outgoing lines of the power supply path are different from each other, since the estimate is made after the cell arrangement is completed, there is no problem. In other words, since the estimate is made after the cell arrangement is completed, correlation of the configurations and dimensions of the outgoing lines can be various.

However, in recent years, a high-performance and sophisticated system has been increasingly developed. Accordingly, referring to the estimate for the charge and discharge times and power consumption, it is necessary that the estimate be made at an early stage of the design process instead of being made after the cell arrangement is completed.

## SUMMARY OF THE INVENTION

It is an object of the present invention to provide a structure of a power supply path utilized in the design of an integrated circuit in which an estimate for charge and discharge times and power consumption of a part to be controlled can be made at a stage before cell arrangement is completed.

In order to solve the above problems, according to a structure of a power supply path utilized in the design of an integrated circuit of the present invention, the pitches between adjacent outgoing lines of a plurality of outgoing lines branching off from a main line of a power supply path are set so as to be equal to each other in each of the power supply paths both on the power supply side of a high potential and the power supply side of a low potential.

Thus, resistance values and stray capacitance values of all elements of the main line provided between the adjacent outgoing lines become constant values (standard values), respectively. Therefore, charge and discharge times and power consumption of a part to be controlled can be advantageously and accurately estimated before cell arrangement is completed.

According to a preferred embodiment of the present invention, branching positions of the plural outgoing lines of the power supply path on the power supply side of the high potential correspond to branching positions of the plural outgoing lines of the power supply path on the power supply side of the low potential in the longitudinal direction of the power supply paths.

Thus, influences of the existence of the outgoing lines of the power supply path on the power supply side of the high potential, applied to the stray capacitance values of the elements in the main line and the outgoing lines of the power supply path on the power supply side of the low potential can be equalized. Furthermore, influences of the existence of the

outgoing lines of the power supply path on the power side of the low potential, applied to the stray capacitance values of the elements in the main line and the outgoing lines of the power supply path on the power supply side of the high potential can be equalized. As a result, charge and discharge times and power consumption of a part to be controlled can be advantageously estimated before cell arrangement is completed.

According to still another embodiment of the present invention, lengths of the outgoing lines are set so as to be equal to each other in both the power supply paths on the power supply sides of the high potential and the low potential, respectively.

Thus, the resistance values and stray capacitance values of all outgoing lines can be equal to each other, respectively. As a result, charge and discharge times and power consumption of a part to be controlled can be advantageously estimated before cell arrangement is completed.

According to still another embodiment of the present invention, the lengths of the plural outgoing lines of the power supply path on the power supply side of the high potential are set so as to be longer than the lengths of the plural outgoing lines of the power supply path on the power supply side of the low potential.

Thus, a clear distinction can be made with respect to resistance values and stray capacitance values of the outgoing lines between the power supply path on the power supply side of the high potential and that on the power supply side of the low potential. As a result, charge and discharge times and power consumption of a part to be controlled can be advantageously estimated before cell arrangement is completed.

According to still another embodiment of the present invention, widths of the respective plural outgoing lines are equal to each other and set so as to be smaller than distances

between the adjacent outgoing lines in both the power supply paths on the power supply sides of the high potential and the low potential, respectively.

5 Thus, resistance values and stray capacitance values of the outgoing lines are equalized. As a result, charge and discharge times and power consumption of a part to be controlled can be advantageously estimated before cell arrangement is completed.

10 It is noted that some or all of the foregoing embodiments can be combined into a single embodiment.

The foregoing and other aspects will become apparent from the following description of the invention when considered in conjunction with the accompanying drawing figures.

#### 15 BRIEF DESCRIPTION OF THE DRAWING FIGURES

FIG. 1 is a plan view showing a structure of a power supply path utilized in the design of an integrated circuit according to a first embodiment of the present invention.

20 FIG. 2 is a plan view showing a structure of a power supply path utilized in the design of an integrated circuit according to a second embodiment of the present invention.

FIG. 3 is a plan view showing a structure of a power supply path utilized in the design of an integrated circuit according to a third embodiment of the present invention.

25 FIG. 4 is a plan view showing a structure of a power supply path utilized in the design of an integrated circuit according to a fourth embodiment of the present invention.

FIG. 5 is a plan view showing a structure of a power supply path for an auxiliary explanation.

30 In all these figures, like components are indicated by the same numerals.

## DETAILED DESCRIPTION

Hereinafter, preferred embodiments of the present invention are described with reference to the drawings.  
(Auxiliary explanation)

Before a description is given of a structure of a power supply path utilized in the design of an integrated circuit according to the embodiments of the present invention, a description is given of a power supply path structure to be premised with reference to FIG. 5 in order to be easily understood.

FIG. 5 is a plan view showing a power supply path structure utilized in the design of an integrated circuit for an auxiliary explanation. This figure illustrates a part in which a power supply is controlled. Referring to FIG. 5, reference numeral 30 designates a power supply path on a power supply VDD side of a high potential, reference numeral 30a designates a main line and reference numerals 31, 32 and 33 designate outgoing lines branching off from the main line 30a, reference numeral 40 designates a power supply path on a power supply VSS side of a low potential, reference numeral 40a designates a main line, and reference numerals 41, 42 and 42 designate outgoing lines branching off from the main line 40a. In FIG. 5, resistance and capacitance as an equivalent circuit are illustrated in a superimposed manner.

Referring to the power supply path 30 on the VDD side, a pitch  $r1$  between the adjacent outgoing lines 31 and 32 does not coincide with a pitch  $r2$  between the adjacent outgoing lines 32 and 33 ( $r1 \neq r2$ ). This is similar in the power supply path 40 on the VSS side ( $s1 \neq s2$ ).

In addition, branching positions of the outgoing lines 31, 32 and 33 are shifted from the branching positions of the outgoing lines 41, 42 and 43 in the longitudinal direction of the power supply paths.

In addition, lengths of the outgoing lines 31, 32 and 33

are not equal and lengths of the outgoing lines 41, 42 and 42 are also not equal.

In addition, referring to the widths of the outgoing lines, a width of the outgoing line 33 is not equal to those of the outgoing lines 31 and 32. Furthermore, a width of the outgoing line 43 is not equal to those of the outgoing lines 41 and 42.

Furthermore, a distance  $t_2$  between the outgoing lines 41 and 42 is smaller than a width  $t_1$  of the outgoing line 41 ( $t_1 > t_2$ ).

Thus, the configurations and dimensions of the outgoing lines of the power supply path in a part to be controlled are different from each other.

When a voltage at a part of an integrated circuit or the whole thereof is controlled, an estimate for charge and discharge times has been made after cell arrangement is completed and the power supply path is determined. In this estimate, a resistance value and a stray capacitance value of a main line, and a resistance value and a stray capacitance value of an outgoing line of the power supply path are comprehensively considered to calculate the charge and discharge times and power consumption. When this estimate is made after cell arrangement is completed and the power supply path is determined, it is all right if configurations and dimensions of the outgoing lines of the power supply path are different from each other. However, in recent years, a high-performance and sophisticated system has been increasingly developed and accordingly, it is very important to estimate the charge and discharge times and power consumption at an early stage of designing.

Hereinafter, a description is given of a structure of a power supply path utilized in the design of an integrated circuit according to preferred embodiments of the present invention with reference to the drawings.

(First embodiment)

FIG. 1 is a plan view showing a structure of a power supply path utilized in the design of an integrated circuit according to a first embodiment of the present invention.

Referring to FIG. 1, reference numeral 10 designates a power supply path on the side of VDD, reference numeral 10a designates a main line, reference numerals 11, 12 and 13 designate outgoing lines branching off from the main line 10a, reference numeral 20 designates a power supply path on the side of VSS, reference numeral 20a designates a main line, and reference numerals 21, 22 and 23 designate outgoing lines branching off from the main line 20a.

Referring to the outgoing lines 11, 12 and 13 of the power supply path 10 on the side of VDD, pitches P1 and P2 between their branching positions are equal to each other ( $P1 = P2$ ). Similarly, referring to the outgoing lines 21, 22 and 23 of the power supply path 20 on the side of VSS, pitches Q1 and Q2 between their branching positions are equal to each other ( $Q1 = Q2$ ).

In other words, the pitches between the branching positions of the outgoing lines are constant on the sides of VDD and VSS, respectively. In addition, according to the illustrated example, it is satisfied that  $P1 = P2 = Q1 = Q2$ .

Furthermore, in this embodiment of the present invention, a relation of lengths of the outgoing lines between the power supply path on the side of VDD and the power supply path on the side of VSS is not an issue, and neither is a relation of lengths of the plural outgoing lines on the same power supply path.

According to this embodiment, the outgoing lines on the power supply path are disposed at the same pitch and referring to elements 10a<sub>1</sub> and 10a<sub>2</sub> or 20a<sub>1</sub> and 20a<sub>2</sub> of the main line between the adjacent outgoing lines, since a resistance value and a stray capacitance value of each element of the main line are constant values (standard values), respectively, charge and discharge times and power consumption of a part to be controlled can be

advantageously and accurately estimated before the cell arrangement is completed.

(Second embodiment)

FIG. 2 is a plan view showing a structure of a power supply path utilized in the design of an integrated circuit according to a second embodiment of the present invention.

According to this embodiment, branching positions of outgoing lines 11, 12 and 13 in a power supply path 10 on the side of VDD correspond to branching positions of the outgoing lines 21, 22 and 23 in a power supply path 20 on the side of VSS in the longitudinal direction of the power supply paths. As is clear from FIGs. 1 and 2, the upper and lower power supply paths are shifted in the lateral direction in FIG. 1 while there is no such a shift in FIG. 2. Since the constitution is the same as the first embodiment shown in FIG. 1 except for this point, the same part is allotted to the same reference numeral or sign and its description is omitted.

In addition, a relation of lengths of the outgoing lines between the power supply path on the side of VDD and the power supply path on the side of VSS is not an issue in this embodiment.

According to this embodiment, influences of the existence of the outgoing lines 11, 12 and 13 of the power supply path 10 on the side of VDD, applied to the stray capacitance values of the elements  $20a_1$  and  $20a_2$  in the main line and the outgoing lines 21, 22 and 23 of the power supply path 20 on the side of VSS can be equalized. Furthermore, influences of the existence of the outgoing lines 21, 22 and 23 of the outgoing line 20 on the side of VSS, applied to the stray capacitance values of the elements  $10a_1$  and  $10a_2$  in the main line and the outgoing lines 11, 12 and 13 of the power supply path 10 on the side of VDD can be equalized. As a result, charge and discharge times and power consumption of a part to be controlled can be advantageously and accurately estimated before cell arrangement is completed.



(Third embodiment)

FIG. 3 is a plan view showing a structure of a power supply path utilized in the design of an integrated circuit according to a third embodiment of the present invention.

According to this embodiment, referring to a relation of lengths of outgoing lines, lengths of outgoing lines 11, 12 and 13 of a power supply path 10 on the side of VDD are each equal to  $d1$  and also, lengths of outgoing lines 21, 22 and 23 of a power supply path 20 on the side of VSS are each equal to  $d2$ . Furthermore, the length  $d1$  of each of the outgoing lines 11, 12 and 13 is set so as to be longer than the length  $d2$  of each of the outgoing lines 21, 22 and 23 ( $d1 > d2$ ). Since the constitution is the same as that of the second embodiment shown in FIG. 2 except for this point, the same part is allotted to the same reference numeral or sign and its description is omitted.

According to this embodiment, since a clear distinction can be made between resistance values and stray capacitance values of the outgoing lines 11, 12 and 13 of the power supply path 10 on the side of VDD, and resistance values and stray capacitance values of the outgoing lines 21, 22 and 23 of the power supply path 20 on the side of VSS, charge and discharge times and power consumption of a part to be controlled can be advantageously and accurately estimated before cell arrangement is completed.

In addition, it is preferable that this embodiment comprise the structures of the first and second embodiments.

(Fourth embodiment)

FIG. 4 is a plan view showing a structure of a power supply path utilized in the design of an integrated circuit according to a fourth embodiment of the present invention.

According to this embodiment, a width  $W1$  of each outgoing lines 11, 12 and 13 is set so as to be shorter than a distance  $W2$  between the outgoing lines in a power supply path 10 on the

side of VDD ( $W1 < W2$ ). In addition, a width  $W3$  of each of outgoing lines 21, 22 and 23 is set so as to be shorter than a distance  $W4$  between the outgoing lines in a power supply path 20 on the side of VSS ( $W3 < W4$ ). Furthermore, it is preferable that  $W1 = W3$  and  $W2 = W4$ . Since the constitution is the same as that of the third embodiment shown in FIG. 3 except for this point, the same part is allotted to the same reference numeral or sign and its description is omitted.

According to this embodiment, since resistance values and stray capacitance values of the outgoing lines can be equalized, charge and discharge times and power consumption of a part to be controlled can be advantageously estimated before cell arrangement is completed.

Furthermore, it is preferable that this embodiment comprises the structures of the first and second embodiments, or the structures of the first and third embodiments.

According to the present invention as described above, referring to the plurality of outgoing lines of the power supply path on the power supply side of a high potential and the plurality of outgoing lines of the power supply path on the power supply side of a low potential, since their pitches, lengths and widths are equalized, the resistance values and the stray capacitance values of the elements of the main line and outgoing lines in each power supply path can be equalized. As a result, the charge and discharge times and power consumption of the parts to be controlled can be advantageously estimated before the cell arrangement is completed.

From the above description, it will be apparent what the present invention provides.